REMARKS

The Examiner's Office Action dated on November 10, 2003 has been received and its contents carefully considered.

Claims 1-16 are pending in this application. Claims 10-16 are canceled without waiver or prejudice. Claims 1-9 are amended, and new claims 17-30 are added. No new matter is added. Claims 1, 4, 17, 29, and 30 are independent claims.

The specification has been amended to correct typographical and idiomatic errors noted by Applicants during review of the application. No new matter is added.

Objections to claims 2-3

Claims 2-3 stand objected to because of the informalities that they are duplicate of each other. Claims 2-3 have been amended to correct the informalities. It is respectfully submitted that the objections be withdrawn.

Rejection of claim 9 under 35 U.S.C. §112

Claim 9 stands rejected under 35 U.S.C. §112, second paragraph, as set forth on page 2 of the Office Action. Claim 9 has been amended to be dependent upon claim 5 so that there is sufficient antecedent basis for the limitation "said XOR" in line 4 of claim 9. In addition, claim 9 has been amended to correct typographical and idiomatic errors noted by the Applicants during review of the application. Withdrawal of the rejection is respectfully requested.

Allowance of claims

Applicants acknowledge with appreciation the Examiner's indication in the Office Action that claims 5-8 would be allowable if rewritten in independent form including all features of the base claim and any intervening claims, and that claim 9 would be allowable if rewritten to overcome the rejection under 35 U.S.C. §112,

second paragraph, set forth in the Office Action and to include all of the features of the base claim and any intervening claims.

Applicants have elected to accomplish an equivalent result to make claims 5-9 allowed by rewriting claim 5 into new independent claim 17 and rewriting claims 6-9 into new dependent claims 18-21 of claim 17, respectively, wherein the features recited in original claims 4 and 5 are incorporated into claim 17. In particular, claim 9 has been rewritten into claim 21 to overcome the rejection under 35 U.S.C. §112, second paragraph by making claim 21 dependent upon claim 17, wherein typographical and idiomatic errors of claim 9 noted by Applicants are corrected. Therefore, Applicants respectfully submit that claims 17-21 are now placed in condition for allowance.

Rejections of claims 1-4 under 35 U.S.C. §102(b)

Claims 1-4 stand rejected under 35 U.S.C. §102(b) as anticipated by U.S. Pat. No. 5,764,173 to Flynn (hereinafter, called *Flynn*).

The Office Action alleges that "[R]egarding claims 1-4, *Flynn* discloses a driving circuit and a corresponding method for converting digital sound data into corresponding driving signals to drive a speaker (col. 3, lines 43-49), the digital sound data is being divided into a higher bits data group (8 as shown in FIG. 1) and a lower bits data group (6 as shown in Fig. 1), the circuit comprising a pulse width modulation circuit (12 in Fig. 2) and a pulse height conversion circuit (14 in Fig. 2)." Applicants respectfully traverse the rejections.

Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. Thus, every claimed feature must be represented in the applied reference to constitute a proper rejection under 35 U.S.C.

§102(b). For the reasons set forth below, Applicants respectfully assert that the *Flynn* reference does not disclose, teach, or suggest all elements of claims 1-4, as amended.

Regarding amended claim 1

Applicants' independent claim 1, as amended, recites (*emphasis added*):

1. A driving method of speaker for converting digital sound data into corresponding driving signals to drive said speaker, the driving method comprising the steps of:

dividing said digital sound data into at least two data groups, including a first data group and a second data group;

modulating said first data group into a first driving signal, wherein the magnitude of said first data group is represented by pulse width of said first driving signal;

converting a first input signal based on said second data group into a second driving signal according to said second data group and under the control of a second input signal based on said first driving signal, wherein the magnitude of said second data group is represented by pulse height of said second driving signal;

outputting a speaker driving signal according to at least said second driving signal; and

driving said speaker according to said speaker driving signal.

With regard to claim 1, the Office Action recites that *Flynn* discloses "a corresponding method for converting digital sound data into corresponding driving signals to drive a speaker". Applicants respectfully submit that the recitation is

improper for at least the reason that *Flynn* fails to teach the claim language highlighted in amended claim 1 above.

Specifically, elements 12 and 14 in FIG. 2 of the *Flynn* reference are regarded in the Office Action as teaching the features recited in claim 1. According to *Flynn*, elements 12 and 14 are a pulse width modulating decoder and a chord decoder respectively. The *Flynn* reference (col. 5, lines 1-5) recites that "[A] 5-bit pulse width modulating decoder (in fact shared between all the output stages) 12 converts the control field bits 8 to a pulse width modulated signal PWM having one of 32 possible duty cycles." *Flynn* additionally recites that:

> "A chord decoder 14 is responsive to the chord selecting bits 6 to produce a chord-steering output that it is supplied to a multiplexer 16. Depending upon the content of the chord selecting bits 6, the chord decoder 14 controls the multiplexer 16 by the chord-steering bits to select one of an on-signal 18, an off-signal 20, and the pulse width modulated signal for output by the multiplexer 16. The mapping of the chord selecting bits 6 to the chord-steering signal will differ for different output stages such that for any given chord selecting bits, one of the multiplexers will select the Pulse Width Modulated signal, the higher order multiplexers will select the on-signal 18 and the lower order multiplexers will select the off-signal 20." (col. 5, lines 14-26)

In contrast to *Flynn's* teachings, Applicants' claim 1, as amended, recites "**modulating** said first data group into ***a first driving signal***, wherein ***the magnitude of said first data group is represented by pulse width of said first driving signal***"; and "**converting** a first input signal based on ***said second data group*** into ***a second driving signal*** according to ***said second data group*** and ***under the control of a second input***

signal based on said first driving signal, wherein ***the magnitude of said second data group is represented by pulse height of said second driving signal"*** (emphasis added). Accordingly, Applicants assert that the *Flynn* reference fails to anticipate amend claim 1 for at least the reason that *Flynn* does not disclose, teach, or suggest "**converting** a first input signal based on ***said second data group*** into ***a second driving signal*** according to ***said second data group*** and ***under the control of a second input signal based on said first driving signal"***, wherein "***the magnitude of said second data group is represented by pulse height of said second driving signal" and "the magnitude of said first data group is represented by pulse width of said first driving signal"***, as recited in amended claim 1.

Specifically, as shown in FIGS. 2 and 5 of the *Flynn* reference, the chord decoder 14 has the chord selecting bits 6 as input signals, and chord steering signals (i.e. EN[3]~EN[0]) as output signals. However, according to *Flynn's* FIG. 5, the magnitude of the chord selecting bits 6 is not represented by the chord steering signals (i.e. EN[3]~EN[0]) through the chord decoder 14. Thus, *Flynn* does not disclose, teach, or suggest said **converting step**, set forth in amended claim 1, wherein "***the magnitude of said second data group is represented by pulse height of said second driving signal"*** (emphasis added).

Applicants respectfully submits that amended claim 1 is patentably distinguishable over the *Flynn* reference for at least the reasons above and the rejection of claim 1, as amended, should be withdrawn.

Regarding amended claim 4

Applicants' independent claim 4, as amended, recites (emphasis added):

4. A driving circuit of speaker for converting digital sound data into corresponding driving signals to drive said speaker, said digital sound data being divided into at least two data groups including a first data group and a second data group, the driving circuit comprising:

a pulse width modulation circuit being used to modulate said first data group into a first driving signal, wherein the magnitude of said first data group is represented by pulse width of said first driving signal; and

a pulse height conversion circuit being used to convert said a first input signal based on said second data group into a second driving signal according to said second data group and under the control of a second input signal based on said first driving signal, and to output a speaker driving signal according to at least said second driving signal, wherein the magnitude of said second data group is represented by pulse height of said second driving signal;

wherein said speaker is driven according to said speaker driving signal.

In regard to claim 4, the Office Action recites that *Flynn* discloses "a driving circuit and a corresponding method for converting digital sound data into corresponding driving signals to drive a speaker". Applicants respectfully submit that the statement is improper for at least the reason that *Flynn* fails to teach the claim language highlighted in amended claim 4 above.

In particular, the Office Action equates elements 12 and 14 in FIG. 2 of the *Flynn* reference with a pulse width modulation circuit and a pulse height conversion circuit, recited in amended claim 4, respectively. Applicants respectfully traverse this equation for at least the following reason. The *Flynn* reference (col. 5, lines 1-5) recites

that "[A] 5-bit pulse width modulating decoder (in fact shared between all the output stages) 12 converts the control field bits 8 to a pulse width modulated signal PWM having one of 32 possible duty cycles." *Flynn* also recites that:

> "A chord decoder 14 is responsive to the chord selecting bits 6 to produce a chord-steering output that it is supplied to a multiplexer 16. Depending upon the content of the chord selecting bits 6, the chord decoder 14 controls the multiplexer 16 by the chord-steering bits to select one of an on-signal 18, an off-signal 20, and the pulse width modulated signal for output by the multiplexer 16. The mapping of the chord selecting bits 6 to the chord-steering signal will differ for different output stages such that for any given chord selecting bits, one of the multiplexers will select the Pulse Width Modulated signal, the higher order multiplexers will select the on-signal 18 and the lower order multiplexers will select the off-signal 20." (col. 5, lines 14-26)

In contrast to *Flynn's* teachings of element 14, Applicants' claim 4, as amended, sets forth "**a pulse height conversion circuit** being used to convert said a first input signal based on said second data group into a second driving signal according to said second data group and ***under the control of a second input signal based on said first driving signal***, and to output a speaker driving signal according to at least said second driving signal", wherein "***the magnitude of said second data group is represented by pulse height of said second driving signal"*** (emphasis added). Accordingly, Applicants respectfully submit *Flynn*'s element 14 fails to disclose, teach, or suggest the **pulse height conversion circuit** recited in amended claim 4. The *Flynn* reference fails to anticipate amended claim 4 for at least the reason that *Flynn* does not disclose, teach, or suggest **a pulse height conversion circuit**, set forth in amended claim 4.

Specifically, as shown in FIGS. 2 and 5 of the *Flynn* reference, the chord decoder 14 has the chord selecting bits 6 as input signals, and chord steering signals (i.e. EN[3]~EN[0]) as output signals. However, according to *Flynn's* FIG. 5, the magnitude of the chord selecting bits 6 is not represented by the chord steering signals (i.e. EN[3]~EN[0]) through the chord decoder 14. Thus, *Flynn* does not disclose, teach, or suggest **a pulse height conversion circuit**, set forth in amended claim 4, wherein "***the magnitude of said second data group is represented by pulse height of said second driving signal***" (emphasis added).

Applicants respectfully submit that amended claim 4 is patentably distinguishable over the *Flynn* reference and the rejection of amended claim 4 should be withdrawn.

Moreover, no motivation is indicated in the *Flynn* reference for one of ordinary skill in the art to modify the *Flynn*'s teachings to meet Applicants' independent claims 1 and 4. Consequently, it is respectfully submitted that independent claims 1 and 4, as amended, be allowed, and that amended claims 2-3 be allowed for at least the reason that they are dependent upon claim 1, as amended, and the rejections of claims 1-4 be withdrawn.

Objections to claims 5-9

Claims 5-9 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form as indicated in the Office Action. Claims 5-9 have been rewritten as new claims 17-21 to render the allowance of claims 17-21, as discussed above. Consistent with discussion regarding amended claim 4, it is respectfully submitted that claims 5-9 be allowed for at least the reason that claims 5-9

are dependent, directly or indirectly, upon independent claim 4, as amended, and the objections to claims 5-9 be withdrawn.

New claims 22-30

New claims 22-30 are added to further protect the invention in different scope, and are supported by the detailed description of the specification as well as drawings. Thus, no new matter is added. Consistent with discussion regarding amended claims 1 and 4, it is respectfully submitted that claims 22-27, and 28 be allowed for at least the reason that they are dependent, directly or indirectly, upon corresponding base claims 1 and 4, with additional features.

Conclusion

For the foregoing reasons, it is respectfully submitted that this application, as amended, is in condition for allowance. Notice of such allowance and passing of the application to issue, are earnestly requested.

Should the Examiner feel that a conference would be helpful in expediting the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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